NCP3155A, NCP3155B

Product Preview

3 A Synchronous Buck Regulator

The NCP3155 is a DC/DC synchronous switching regulator with fully integrated power switches and full fault protection. The switching frequency of 1 MHz and 500 kHz allows the use of small filter components, which results in smaller board space and reduced BOM cost. Available in a SOIC-8 package.

Features

- Input Voltage Range from 4.7 V to 24 V
- Adjustable Output Voltage
- 1 MHz Operation (NCP3155B – 500 kHz)
- Internally Programmed 4.1 ms Soft−Start
- 0.8 ± 1.0% Reference Voltage
- 100 mΩ HS−FET and 50 mΩ LS−FET
- Current Limit and Short Circuit Protection
- Transconductance Amplifier with External Compensation
- Input Undervoltage Lockout
- Output Overvoltage and Undervoltage Detection
- This is a Pb−Free Device

Typical Applications

- Set Top Boxes
- DVD Drives and HDD
- LCD Monitors and TVs
- Cable Modems
- Telecom/Networking/Datacom Equipment

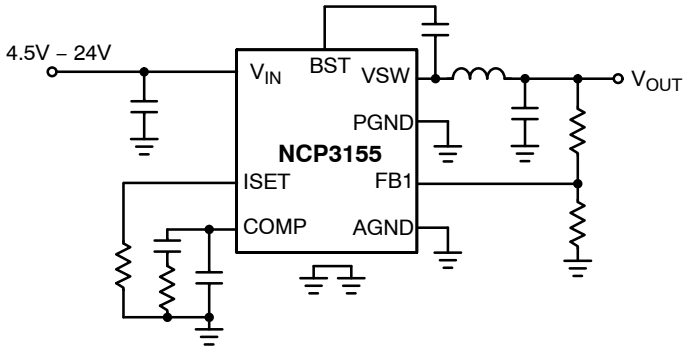

Figure 1. Typical Application Circuit

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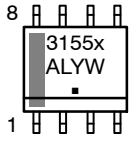
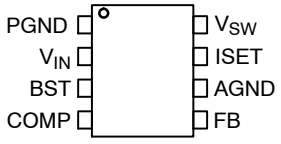
SOIC−8 NB
CASE 751

MARKING DIAGRAM



3155x	= Specific Device Code
	x = A or B
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP3155ADR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP3155BDR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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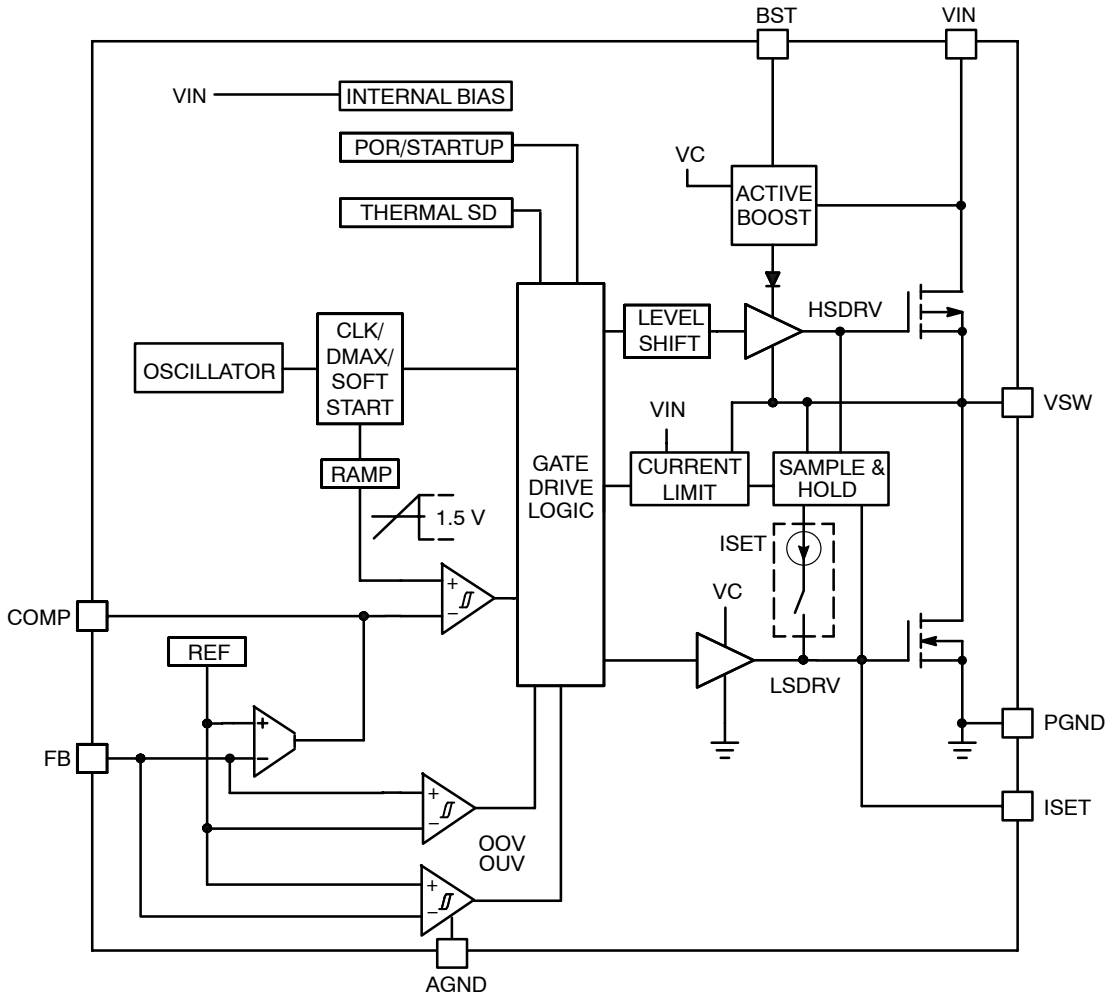


Figure 2. NCP3155 Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Pin Name	Description
1	PGND	The PGND pin is the high current ground pin for the lower MOSFET and drivers which should be soldered to a large copper area to reduce thermal resistance.
2	V_{IN}	The V_{IN} pin powers the internal control circuitry and is monitored by an undervoltage comparator. The V_{IN} pin is also connected to the internal power NMOS switch. It is also used in conjunction with the V_{SW} pin to sense current in the high side MOSFET. The V_{IN} pin has high dI/dt edges and must be decoupled to PGND pin close to the pin of the device.
3	BST	Supply rail for the floating top gate driver. Connect a capacitor (CBST) between this pin and the V_{SW} pin. Typical values for CBST range from 1 nF to 10 nF.
4	COMP	Compensation pin. The comp pin is the output of the transconductance amplifier and the non−inverting input of the PWM comparator. The comp pin in conjunction with the FB pin are used to compensate the voltage−control feedback loop.
5	FB	Inverting input to the Operational Transconductance Amplifier (OTA). The FB pin in conjunction with the external compensation serves to stabilize and achieve the desired output voltage with voltage mode compensation.
6	AGND	The AGND pin serves as small−signal ground. All small−signal ground paths should connect to the AGND pin at a single point to avoid any high current ground returns.
7	ISET	Bottom gate MOSFET driver pin and the internal current set pin. Place a resistor to ground to set the current limit of the converter.
8	V_{SW}	The V_{SW} pin is the connection of the drain and source of the internal N MOSFETS. The V_{SW} pin swings from V_{IN} when the high side switch is on to small negative voltages when the low side switch is on with high dV/dt transitions.

ABSOLUTE MAXIMUM RATINGS (measured vs. GND pin 8, unless otherwise noted)

Rating	Symbol	V_{MAX}	V_{MIN}	Unit
Main Supply Voltage Input	V_{CC}	26.4	−0.3	V
Boost to V_{SW} differential voltage	BST−V_{SW}	13.2	−0.3	V
High Side Drive Boost Pin	BST	45	−0.3	V
Switch Voltage Node	V_{SW}	30	−0.6	V
Transconductance Amplifier Output	COMP	5.5	−0.3	V
Feedback	FB	6.0	−0.3	V
Current Limit Set	ISET	13.2	−0.3	V
Operating Junction Temperature Range (Note 1)	T_J	−40 to +140		°C
Maximum Junction Temperature	$T_{J(MAX)}$	+150		°C
Storage Temperature Range	T_{stg}	−55 to +150		°C
Thermal Characteristics SOIC−8 Plastic Package (Note 2) Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction−to−Air Linear Derating Factor	 PD $R_{\theta JA}$ 	 TBD TBD TBD		 W °C/W mW/°C
Lead Temperature Soldering (10 sec): Reflow (SMD styles only) Pb−Free (Note 3)	R_F	260 Peak		°C
Moisture Sensitivity Level (Note 4)	MSL	3		
ESD Withstand Voltage (Note 5) Human Body Model Machine Model	V_{ESD}	 2.0 200		 kV V
Latch−up Current (T_A = 85°C) (Note 6)	Lu	+100		mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

2. When mounted on minimum recommended FR−4 or G−10 board
3. 60−180 seconds minimum above 237°C.
4. Moisture Sensitivity Level (MSL): 3 per IPC/JEDEC standard: J−STD−020A.
5. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) per JEDEC standard: JESD22−A114.
   Machine Model (MM) per JEDEC standard: JESD22−A115.
6. Latch−up Current Maximum Rating: per JEDEC standard: JESD78.

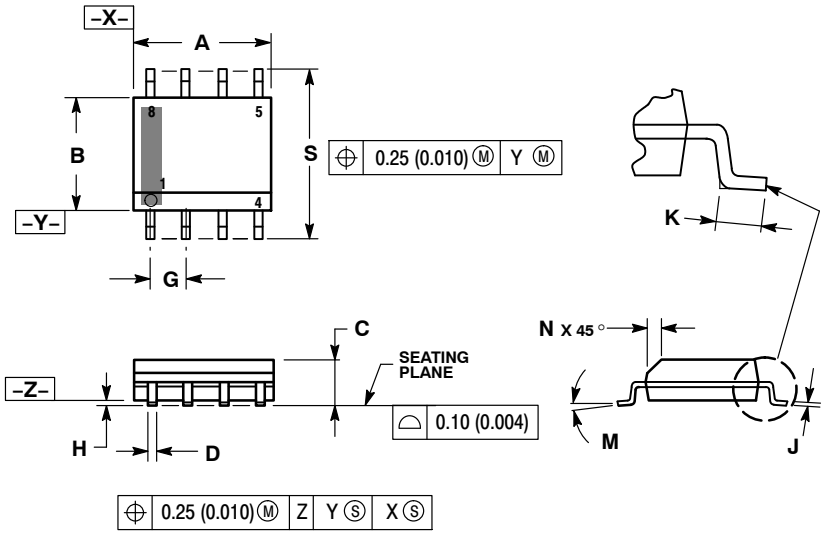
ELECTRICAL CHARACTERISTICS ($-40°C < T_J < +125°C$, V_{CC} = 12 V, for min/max values unless otherwise noted)

Characteristic		Conditions	Min	Typ	Max	Unit
Input Voltage Range		–	4.7		24	V
SUPPLY CURRENT						
V_{CC} Supply Current	NCP3155A	V_{FB} = 0.55 V, Switching, V_{CC} = 4.7 V	–	TBD	TBD	mA
		V_{FB} = 0.55 V, Switching, V_{CC} = 24 V	–	TBD	TBD	mA
V_{CC} Supply Current	NCP3155B	V_{FB} = 0.55 V, Switching, V_{CC} = 4.7 V	–	TBD	TBD	mA
		V_{FB} = 0.55 V, Switching, V_{CC} = 24 V	–	TBD	TBD	mA
UNDER VOLTAGE LOCKOUT						
UVLO Rising Threshold		V_{CC} Rising Edge	4.0	4.3	4.7	V
UVLO Falling Threshold		V_{CC} Falling Edge	3.5	3.9	4.3	V
OSCILLATOR						
Oscillator Frequency	NCP3155A	T_J = +25°C, 4.7 V ≤ V_{CC} ≤ 28 V	830	1000	1170	kHz
		T_J = −40°C to +125°C, 4.7 V ≤ V_{CC} ≤ 28 V	820	1000	1180	kHz
Oscillator Frequency	NCP3155B	T_J = +25°C, 4.7 V ≤ V_{CC} ≤ 28 V	415	500	585	kHz
		T_J = −40°C to +125°C, 4.7 V ≤ V_{CC} ≤ 28 V	400	500	600	kHz
Ramp−Amplitude Voltage		$V_{peak} - V_{alley}$	–	1.5	–	V
Ramp Valley Voltage			0.46	0.71	0.85	V
PWM						
Minimum Duty Cycle		(Note 7)	–	7.0	–	%
Maximum Duty Cycle			80	84	–	%
Soft Start Ramp Time	NCP3155A NCP3155B	$V_{FB} = V_{COMP}$	– –	4.1 4.1	– –	ms
ERROR AMPLIFIER (GM)						
Transconductance			0.9	1.3	1.7	mS
Open Loop dc Gain		(Notes 7 and 9)	–	70	–	dB
Output Source Current		V_{FB} = 545 mV	45	70	100	μA
Output Sink Current		V_{FB} = 655 mV	45	70	100	μA
FB Input Bias Current			–	0.5	500	nA
Feedback Voltage		TJ = 25 C 4.7 V < V_{IN} < 28 V, −40°C < T_J < +125°C	0.792 0.784	0.8 0.8	0.808 0.816	V V
COMP High Voltage		V_{FB} = 0 V	4.0	4.4	5.0	V
COMP Low Voltage		V_{FB} = 2.0 V	–	72	250	mV
OUTPUT VOLTAGE FAULTS						
Feedback OOV Threshold			0.91	1.00	1.09	V
Feedback OUV Threshold			0.56	0.60	0.64	V
PWM OUTPUT STAGE						
High−Side Switch On Resistance		V_{IN} = 12 V V_{IN} = 4.7 V	– –	60 80	75 100	mΩ
Low−Side Switch On Resistance		V_{IN} = 12 V V_{IN} = 4.7 V	– –	36 45	40 50	mΩ
OVERCURRENT						
ISET Source Current			–	12.5	–	μA
Current Limit Set Voltage (Note 8)		R_{SET} = 22.5 kΩ	–	298	–	mV
THERMAL SHUTDOWN						
Thermal Shutdown		(Notes 7 and 10)	–	175	–	°C
Hysteresis		(Notes 7 and 10)	–	20	–	°C

7. Guaranteed by design.
8. The voltage sensed across the high side MOSFET during conduction.
9. This assumes 100 pF capacitance to ground on the COMP Pin and a typical internal R_o of > 10 MΩ.
10. This is not a protection feature.

PACKAGE DIMENSIONS

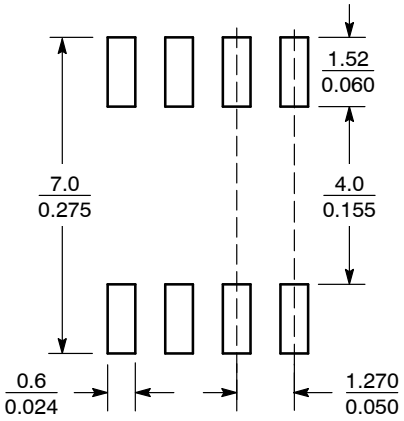
SOIC−8 NB
CASE 751−07
ISSUE AJ



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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